

FIGURE 1

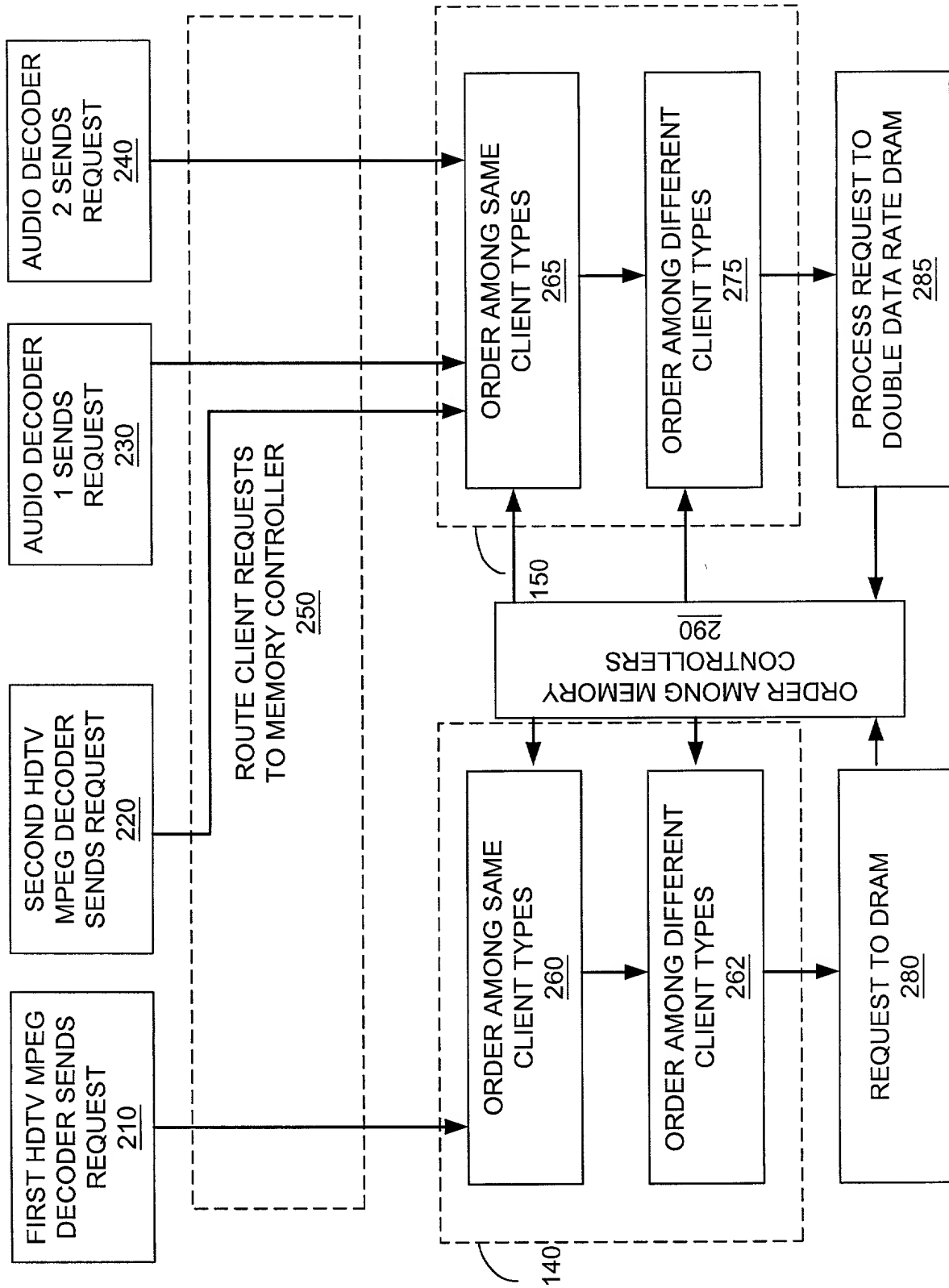
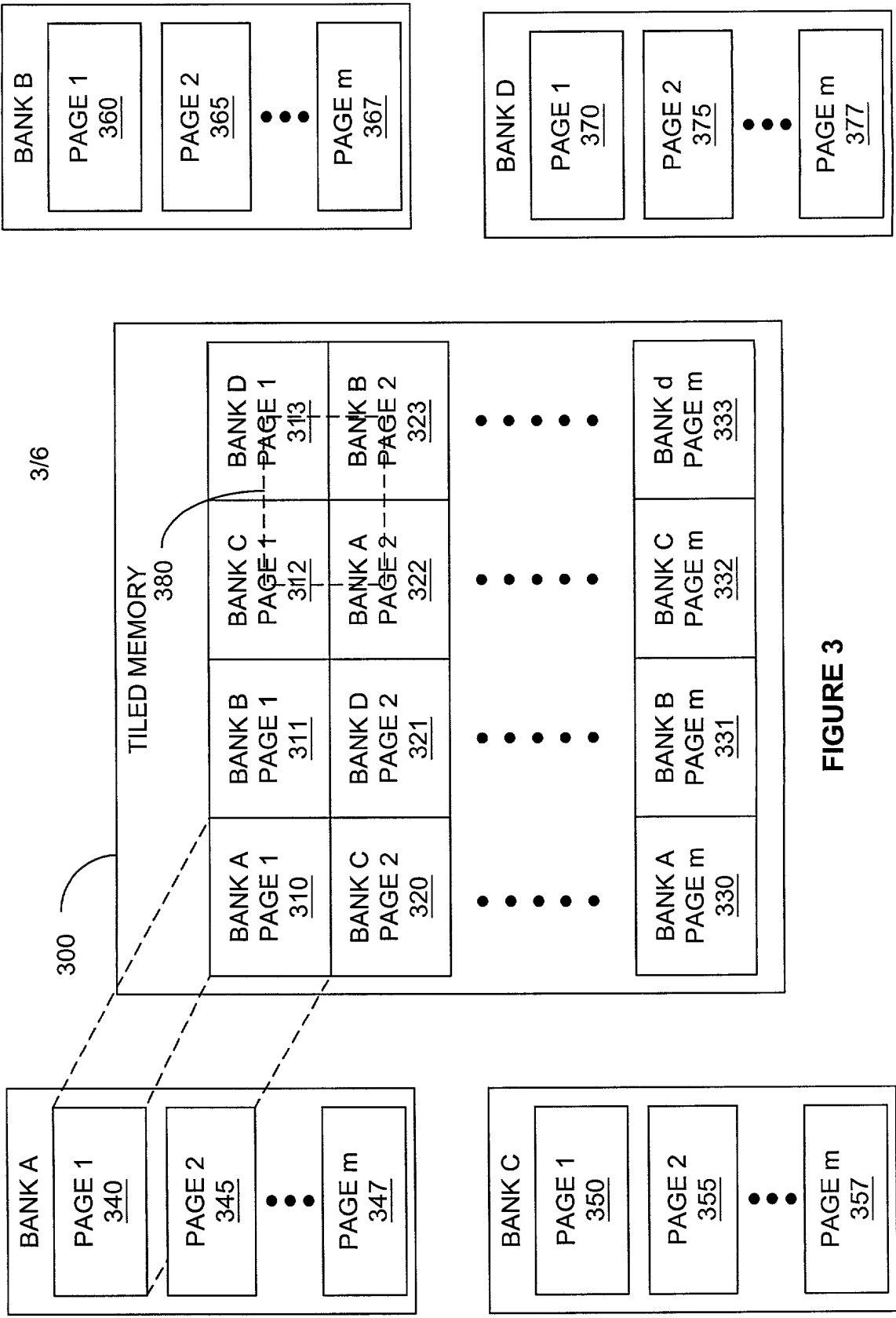


FIGURE 2



**FIGURE 3**

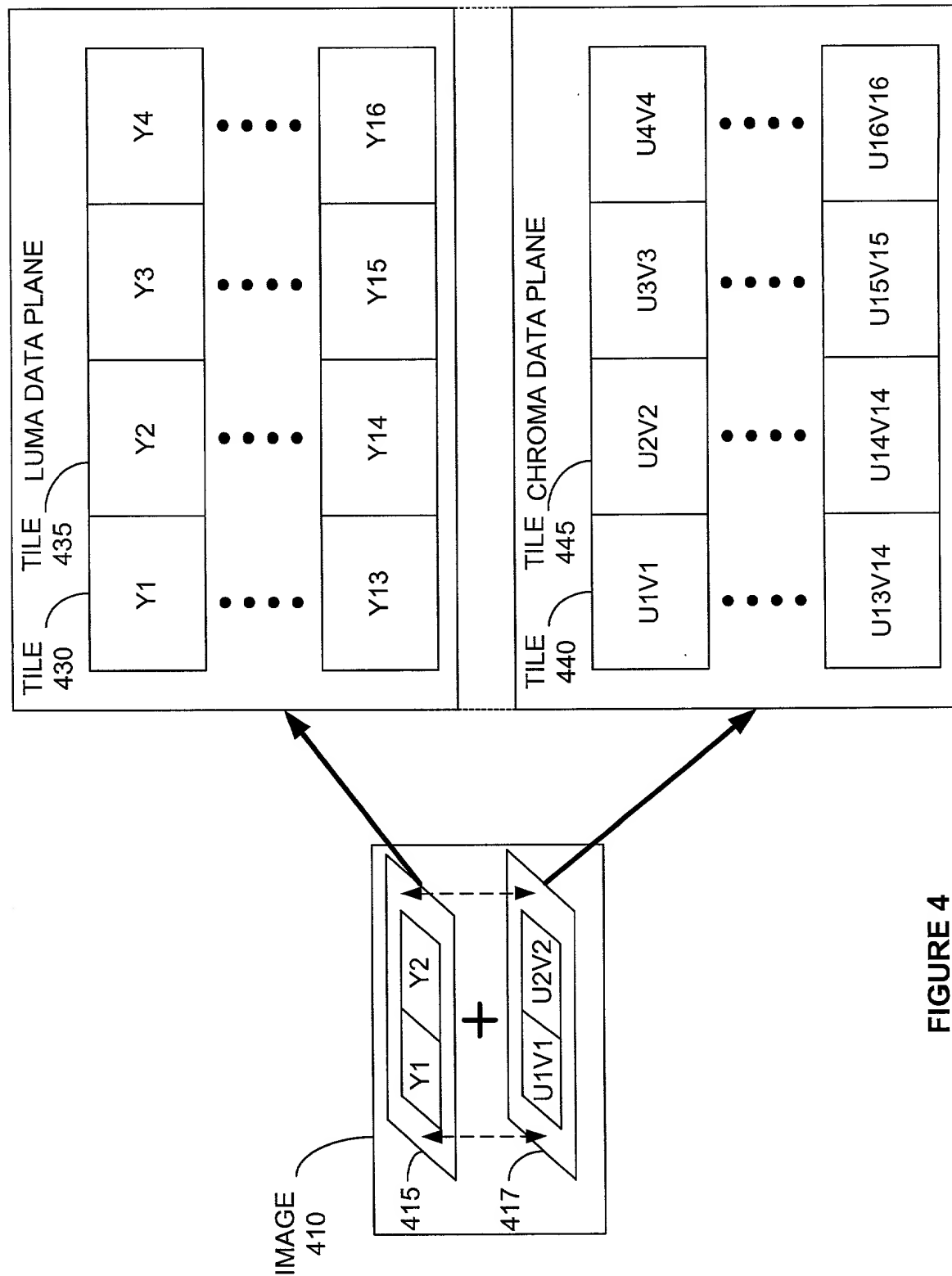


FIGURE 4

A1	B1	C1	D1
C2	D2	A2	B2
A3	B3	C3	D3
C4	D4	A4	B4
C5	D5	A5	B5
A6	B6	C6	D6
C7	D7	A7	B7
A8	B8	C8	D8

415

417

FIGURE 5

FIG. 6 is a block diagram of a video processing system. The system includes a video input source 660, a video processing unit 680, and a video output source 682. The video input source 660 is connected to the video processing unit 680, which is connected to the video output source 682. The video processing unit 680 includes a video buffer 684 and a video processor 686. The video buffer 684 is connected to the video processor 686, which is connected to the video output source 682. The video buffer 684 includes a video buffer 684a and a video buffer 684b. The video buffer 684a is connected to the video processor 686, which is connected to the video output source 682. The video buffer 684b is connected to the video processor 686, which is connected to the video output source 682.

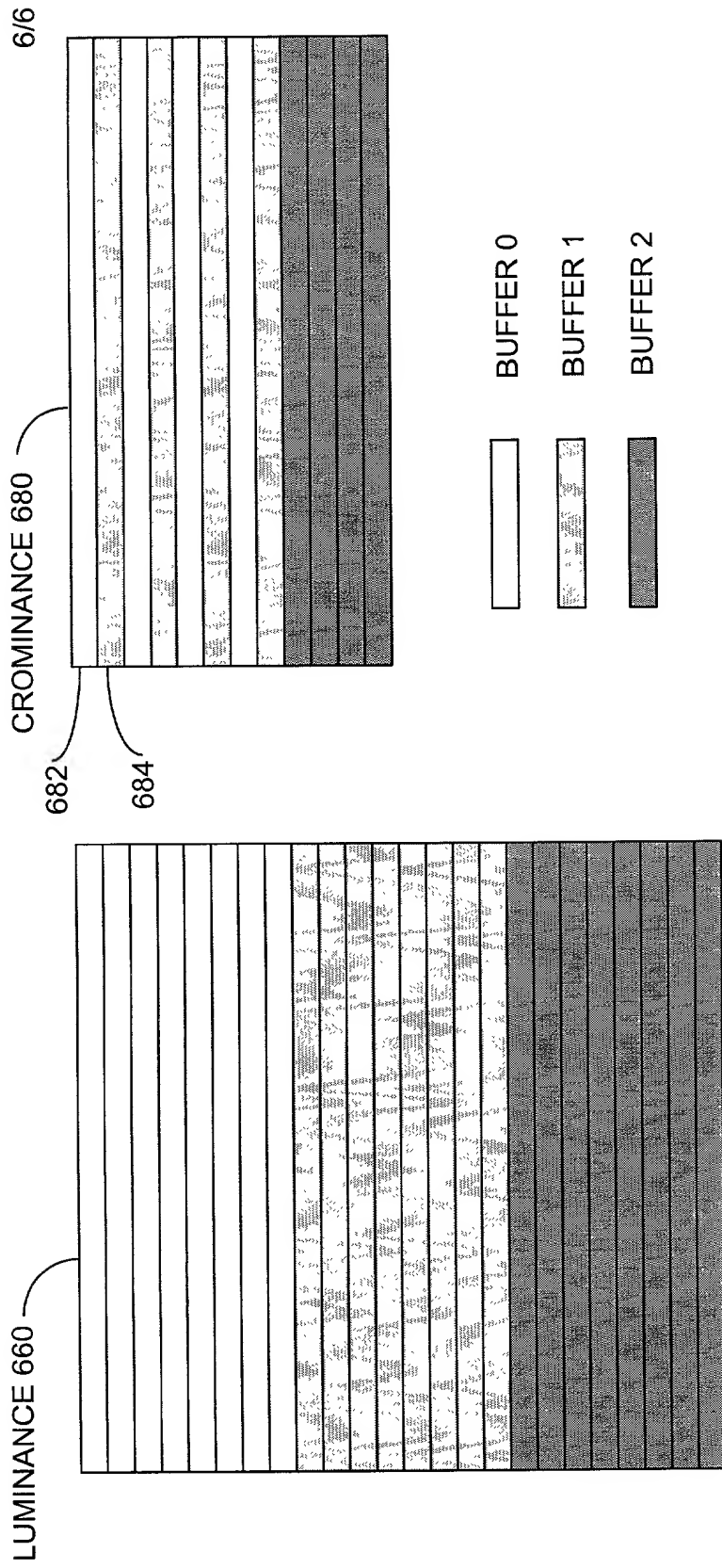


FIGURE 6